DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 17, 2012 has been entered.

Election/Restrictions

Applicant's election of Group I claims 1-33 in the reply filed on October 14, 2010 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 34-135 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

Response to Arguments

Applicant's arguments with respect to Linliu, filed January 17, 2012, have been fully considered but they are not persuasive. As such the rejection as previously set forth is maintained and is repeated below.

Applicant argues that Linliu et al. do not teach the step of transferring the resulting conformal layer structure to the substrate by etching. In support of this position applicant states: "One can clearly see from Fig. 6 ... that the structure of the asserted "thin conformal layer" (210) does not correspond to that of the asserted "top layer" (130)."

For the reasons set forth below, the examiner respectfully disagrees. Annotated versions of Linliu's figures 4 and 7 are shown below. The claimed conformal layer structure is depicted in figure 4. The annotation includes six pairs of dotted lines to emphasize each of the six features of the conformal layer structure that are depicted in figure 4. Also, the left most pair of features is filled in with black shading. Figure 7 of Linliu, which depicts the claimed nanostructure fabricated in the top layer, is shown immediately below figure 4 and figure 7 has been annotated with the same dotted lines and shading scheme as was used for figure 4. The examiner contends that the structure of layer 130 as depicted in figure 7 does in fact correspond to the structure of the conformal layer as depicted in figure 4. It is especially noteworthy that the spacings a/2 and 3a/2 that are shown in each of figures 4 and 7 are the same in each figure.

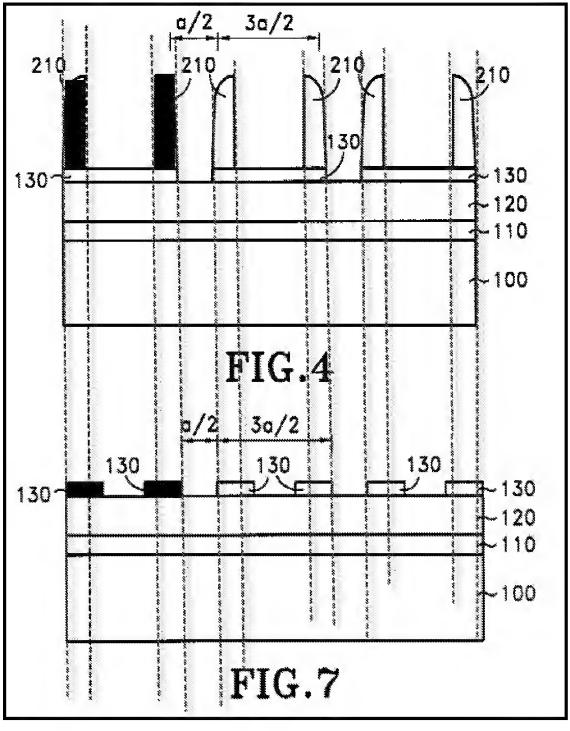
a/2
3a/2
210
210
210
210
130
130
130
120
110
100

FIG.4

a/2
3a/2
130
130
130
130
130
120
110
100

FIG.7

Applicant's arguments with respect to Pontis, filed January 17, 2012, have been fully considered but they are not persuasive with respect to claims 1, 10-12, 14-17, 24, 25, and 30. As such the rejection of these claims as previously set forth is maintained and is repeated below.

Applicant argues that Pontis nanostructures eventually formed by Pontis are nanowire elements 626 and 628 which are composed of the material below the nitride layer 608 (Figs. 6K and 6L). As such Pontis et al. do not teach depositing a sacrificial layer having a first etching characteristic directly on the top layer. The examiner acknowledges that the method of Pontis does proceed to the point where nanowire elements 626 and 628 are fabricated and from a material that is below the nitride layer 608. Nevertheless, Pontis teaches a method that produces the structure depicted in figure 6J wherein features 622 and 624 correspond to the claimed nanostructure that is fabricated in and from the top nitride layer 608 of the substrate.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Claim 13 is dependent upon claim 1. However, claim 13 presents a further limitation that is not allowed by the limitations set forth in claim 1. Claim 1 requires the forming a nanostructure in the top layer of a substrate and claim 1 also requires placing a sacrificial layer directly upon the top layer of the substrate. As such, the further limitation of claim 13 which requires the provision of a protective layer underneath the sacrificial layer requires an intervening layer such that the sacrificial layer would not be placed directly upon the top layer as is required by claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10-14, 17, 22-24 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 6,110,837 issued to Linliu et al. (hereinafter, Linliu).

Regarding claim 1, Linliu teaches a method of fabricating a nanostructure array comprising: providing a substrate (figure 1, 100) having a top layer (figure 1, 120 or

130), and depositing a sacrificial layer having a first etching characteristic, patterning the sacrificial layer (figure 1, 200), forming a thin conformal layer (figure 2, 210) having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern (figure 3), removing the sacrificial layer (figure 4), transferring the resulting conformal layer structure to the substrate by etching, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer (figure 7).

Regarding claim 10, Linliu teaches the substrate is a multilayer structure, comprising: lower layer (100) comprising silicon, an intermediate layer (110) comprising an insulating material, an upper layer (120) comprising a semiconductor (see column 4, lines 12-18).

Regarding claim 11, Linliu teaches the intermediate insulating material is an oxide (see column 4, lines 12-18).

Regarding claim 12, Linliu teaches the upper semiconductor is polysilicon (see column 4, lines 12-18).

Regarding claim 13, Linliu teaches providing a protective layer (figures 1-8, 130 when layer 120 corresponds to the claimed layer) below the sacrificial layer.

Regarding claim 14, Linliu teaches the sacrificial layer is patterned by photolithography (column 4, lines 24-26).

Regarding claim 17, Linliu teaches the sacrificial layer is removed by wet etching (column 4, lines 62-63).

Regarding claims 22 and 23, Linliu teaches the substrate and the top layer comprise the same material (Si) and are separated by an insulator layer (see column 4, lines 12-18).

Regarding claim 24, by virtue of the photolithography process, Linliu teaches at least one nanostructure is fabricated on a predetermined location with positional control.

Regarding claim 30, Linliu teaches the nanostructure comprises the top layer of the substrate (figure 8).

Claims 1 and 10-12, 14-17, 24, 25, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication 2004/0136866 as filed by Pontis et al. (hereinafter, Pontis).

Regarding claim 1, Pontis teaches a method of fabricating a nanostructure array comprising: providing a substrate (figure 6A, 606) having a top layer (figure 6B, 608 or figure 6A, 602), and depositing a sacrificial layer having a first etching characteristic, patterning the sacrificial layer (figure 6E, 610), forming a thin conformal layer (figure 6F, 616) having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern (figure 6G, 618, 620), removing the sacrificial layer (figure 6H), transferring the resulting conformal layer structure to the substrate by etching, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer (figure 6J).

Regarding claims 10-12, Pontis teaches the substrate is a multilayer structure, comprising: a lower layer (606) comprising silicon, an intermediate layer (604) comprising an insulating material, such as an oxide, an upper layer (602) comprising a semiconductor, such as silicon (see [0073]).

Regarding claim 14, Pontis teaches the sacrificial layer is patterned by photolithography ([0073]).

Regarding claim 15, Pontis teaches the conformal layer comprises silicon oxide ([0074]).

Regarding claim 16, Pontis teaches the conformal layer can be formed by chemical vapor deposition, spin coating, sputtering, evaporation or chemical reaction with the sacrificial layer ([0074]).

Regarding claim 17, Pontis teaches the sacrificial layer is removed by wet etching ([0077]).

Regarding claim 24, by virtue of the photolithography process, Pontis teaches at least one nanostructure is fabricated on a predetermined location with positional control ([0050]).

Regarding claim 25, Pontis teaches there are between 1000 and 1 billion nanostructures on the array, which are fabricated on a predetermined location and with positional control ([0114]).

Regarding claim 30, Pontis teaches the nanostructure comprises the portion of the top layer of the substrate that has not been etched away (figure 6K).

Allowable Subject Matter

Claims 2-9, 18-21, 26-29 and 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLAN OLSEN whose telephone number is (571)272-1441. The examiner can normally be reached on M, W and F: 1-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Allan Olsen/
Primary Examiner, Art Unit 1716